Document details

Journal of Engineering Science and Technology
Volume 9, Issue 6, 1 December 2014, Pages 761-773

Open Access

Design of a low latency asynchronous adder using early completion detection (Article)

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Abstract

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A new method for designing completion detection for asynchronous adders is introduced. The new completion detection is based on the property of a carrymerge tree for parallel-prefix adders where a generate bit at one level will have the same value as that in the previous level if there is no carry into the sequence of bits. This method has the advantages of a bundled data approach, allowing the use of single-rail completion detection design methodology, yet it allows the detection of early completion with very minimal gate count overhead. An alternative to "speculative completion," this method has approximately 10% improvement in performance at the costs of a 4% increase in area and a negligible increase in power consumption for Hybrid Skalansky Carry-Select and self-timed Kogge-Stone parallel prefix adders. © School of Engineering, Taylor's University.

Author keywords

Completion detection Parallel prefix adder

ISSN: 18234690
Source Type: Journal
Original language: English
Document Type: Article
Publisher: Taylor's University

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