A simple Neutral-Point Voltage Deviation Minimization Method for Three-Level Inverter-Based Shunt Active Power Filter

Y. Hoon, M.A.M. Radzi, M.K. Hassan, and N.F. Mailah

Abstract — Three-level neutral-point diode clamped (NPC) inverters are becoming increasingly popular in current harmonics mitigation due to their superior advantages over the standard two-level inverters. However, the inherent voltage deviation problems at neutral-point have always been the most annoying features of NPC inverter. Consequently, voltage balancing of DC-link capacitors is made compulsory in such topology, where it is usually achieved through proper switching control. Space vector pulse width modulation (SVPWM) is the most widely applied switching technique in NPC inverter. In this paper, a simple neutral-point voltage deviation control algorithm is proposed to further enhance the performance of SVPWM in minimizing the neutral-point voltage deviation. The proposed algorithm is developed and evaluated in MATLAB / Simulink. Simulation results have confirmed the effectiveness of the proposed algorithm in reducing the inherent voltage deviation problems of NPC inverter to a minimum level.

Keywords - Active power filter; DC-link voltage; multilevel inverter; neutral-point voltage deviation; space vector pulsewidth modulation (SVPWM).

I. INTRODUCTION

Widespread use of nonlinear loads has caused various power quality problems especially high current harmonics, reactive power burden, and low power factor to the power systems. As a result, mitigation of current harmonics and correction of power factor are made compulsory. Shunt active power filter (SAPF) is the most effective mitigation tool which is specifically developed to eliminate current harmonics, where all the undesired current components are removed by injecting opposition currents (simply known as injection currents) back to the power system.

Traditionally, most SAPFs rely on standard two-level inverter. However, three-level inverters which have higher advantages in term of output voltage quality and power losses are proven to be a better alternative [1, 2]. SAPFs based on three-level inverters are indeed more complicated than two-level inverter, where a comprehensive switching control strategy is needed to systematically control the increased amount of switching states and simultaneously balance up the voltage across all the DC-link capacitors. In neutral-point diode clamped (NPC) inverter, the voltage across the splitting DC-link capacitors must be equally maintained as half of the overall DC-link voltage so that a balanced injection current can be generated to properly mitigate the current harmonics.

Among all the available switching strategies [3], space vector pulsewidth modulation (SVPWM) technique is the most desirable choice due to its flexibility in switching sequence design to suit various types of inverter topologies. Generally, SVPWM control technique is accomplished via decent selection and execution of switching states based on Nearest Three Vector (NTV) principle [4-6]. Conventionally, SVPWM relies solely on symmetrical switching sequence with equal dwell time allocation for N-type and P-type vectors to reduce voltage imbalance [6]. However, by depending on SVPWM alone is not good enough to completely solve the severe voltage deviation problems of NPC inverter especially when it operates as SAPF. Moreover, fixed dwell time allocation approach is not able to deal with system variations due to inconsistency in electronic components. Although various balancing techniques based on voltage feedback control [5, 7-9] have been proposed to mitigate the problems, they are mostly implemented with high complexity.

Therefore, this paper presents a simple neutral-point voltage deviation control algorithm which is able to reduce the neutral-point voltage deviation of three-phase three-level NPC inverter-based SAPF to a minimum level. The design concept and the effectiveness of the proposed algorithm are verified using MATLAB / Simulink. The remainder of the paper is organized as follows. In Section II, the proposed SAPF with control strategies is explained. Section III presents the details of the SVPWM switching algorithm used in the SAPF. In Section IV, the proposed neutral-point voltage deviation control algorithm is clearly described. The simulation results are presented and discussed in Section V showing the effectiveness of the proposed control algorithm. The paper ends with a brief conclusion in Section VI by summarizing the significant contributions of this work.
II. SHUNT ACTIVE POWER FILTER (SAPF) WITH CONTROL STRATEGIES

Figure 1 shows the three-phase SAPF system utilizing a three-level NPC inverter which is connected at point of common coupling (PCC) between AC source and nonlinear load. On the other hand, the SAPF’s control strategies consist of harmonics extraction algorithm, synchronizer algorithm, DC-link capacitor voltage regulation algorithm, neutral-point voltage deviation control algorithm, and switching (current control) algorithm.

This paper highlights on neutral-point voltage deviation control algorithm. For harmonics extraction algorithm, synchronous reference frame (SRF) technique [10] is used. Meanwhile, a synchronizer is utilized to provide referencing signal to the harmonics extraction algorithm and DC-link capacitor voltage regulation algorithm governed by proportional-integral (PI) technique [1, 10]. Finally, the switching control is realized through 25 kHz SVPWM switching algorithm.

III. SPACE VECTOR PWM SWITCHING SCHEME
In three-level SVPWM switching scheme [4, 6, 7], 27 vectors which includes 3 zero vectors ($V_0^*$), 12 small vectors ($V_1^*$ to $V_6^*$), 6 medium vectors ($V_7^*$ to $V_{12}^*$) and 6 large vectors ($V_{13}^*$ to $V_{18}^*$) are used to construct the space vector diagram as shown in Figure 2(a). Each vector consists of three types of switching states N, O, and P which corresponds to the operating status of an inverter summarized in Table I.

### TABLE I. SWITCHING STATES REPRESENTATION FOR A TYPICAL THREE-LEVEL INVERTER

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Inverter switching status (phase A)</th>
<th>Terminal Voltage ($V_{dd}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>low low high high</td>
<td>$-V_{dd}/2$</td>
</tr>
<tr>
<td>O</td>
<td>low high high low</td>
<td>0</td>
</tr>
<tr>
<td>P</td>
<td>high high low low</td>
<td>$V_{dd}/2$</td>
</tr>
</tbody>
</table>

The area of the hexagon is separated into six equal triangular sectors (I to VI) with four minor triangular regions (1 to 4) in each of them making the total of 24 regions. It is important to note that small vector has two types of switching patterns (N-type and P-type) and meanwhile zero vector which is located at the centre of the hexagon has all three types of switching patterns.

Figure 2: Three-level space vector diagram: (a) division of sectors and regions and (b) six regions division in Sector I for minimizing the voltage deviation at neutral-point

It has widely been reported in the literature [8, 9, 11, 12] voltage deviation at neutral-point is mainly caused by small and medium vectors. Therefore, in order to minimize the deviation, most of the SVPWM switching sequences are designed based on NTV principle [4-6] in which the three nearest vectors of each region are used to generate the required equivalent reference vector located in each region. Additionally, region 1 and 2 of each sector are further divided into two sub-regions, making a total of 6 regions as shown in Figure 2(b). The idea is to achieve a symmetrical switching operation by equally distributing the dwell time between N-type and P-type switching patterns of small vectors over a sampling period $T_s$. At any instance, if $V_{ref}$ is located at region 4 of sector I (sector I-4), a symmetrical eight-segment switching sequence which is designed based on NTV principle can be summarized as Table II. Meanwhile, the dwell time for each vector involved is determined based on volt-second balancing [4, 6] approach given as equation (1).

$$V_{14}T_a + V_7T_b + V_2T_c = V_{ref}T_s$$

$$T_a + T_b + T_c = T_s$$

(1)

where $T_a$, $T_b$, and $T_c$ are the dwell times for $V_{14}$, $V_7$ and $V_2$ respectively.

Consequently, the resulting dwell time for three nearest vectors of sector I-4 is given as
where \( m_a \) is the modulation index defined according to six-step mode operation [13, 14] represented as

\[
m_a = \frac{V_{\text{ref}}}{V_{\text{ref(six-step)}}}; 0 \leq m_a \leq 1
\]

where \( V_{\text{ref}} \) is the fundamental reference voltage generated by the modulator which is equivalent to the radius of the circle shown in Figure 2(a) and \( V_{\text{ref(six-step)}} = \frac{2}{3} V_{dc} \) is the fundamental voltage at six-step operation.

### IV. NEUTRAL-POINT VOLTAGE DEVIATION CONTROL SCHEME

Although the methods of solely applying symmetrical switching sequence with equal dwell time allocation (conventional SVPWM) are reported to have successfully reduced the deviation [6], such approaches are only able to eliminate voltage deviation problems caused by small vectors. The medium vectors are still remaining in SVPWM scheme which is able to response efficiently to instantaneous system conditions is highly essential.

\[
T_a = T_s[2m_a \sin \theta - 1]
\]
\[
T_b = T_s[2m_a \sin \left( \frac{\pi}{3} - \theta \right) \] for \( 0 \leq \theta \leq \pi/3 \)
\[
T_c = T_s[2 - 2m_a \sin \left( \frac{\pi}{3} + \theta \right)]
\]

where \( m_a \) is the modulation index defined according to six-step mode operation [13, 14] represented as

\[
m_a = \frac{V_{\text{ref}}}{V_{\text{ref(six-step)}}}; 0 \leq m_a \leq 1
\]

where \( V_{\text{ref}} \) is the fundamental reference voltage generated by the modulator which is equivalent to the radius of the circle shown in Figure 2(a) and \( V_{\text{ref(six-step)}} = \frac{2}{3} V_{dc} \) is the fundamental voltage at six-step operation.

### TABLE II. SYMMETRICAL EIGHT-SEGMENT SWITCHING SEQUENCE IN SECTOR I-4

<table>
<thead>
<tr>
<th>Segment</th>
<th>Voltage Vector</th>
<th>Switching Pattern</th>
<th>Dwell Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_{2N} )</td>
<td>O</td>
<td>( T_c )</td>
</tr>
<tr>
<td>2</td>
<td>( V_7 )</td>
<td>P</td>
<td>( T_a )</td>
</tr>
<tr>
<td>3</td>
<td>( V_{16} )</td>
<td>P</td>
<td>( T_b )</td>
</tr>
<tr>
<td>4</td>
<td>( V_{17} )</td>
<td>P</td>
<td>( T_a )</td>
</tr>
<tr>
<td>5</td>
<td>( V_{18} )</td>
<td>P</td>
<td>( T_c )</td>
</tr>
<tr>
<td>6</td>
<td>( V_{19} )</td>
<td>P</td>
<td>( T_b )</td>
</tr>
<tr>
<td>7</td>
<td>( V_{20} )</td>
<td>P</td>
<td>( T_c )</td>
</tr>
<tr>
<td>8</td>
<td>( V_{21} )</td>
<td>O</td>
<td>( T_a )</td>
</tr>
</tbody>
</table>

The proposed algorithm is performed by systematically altering the incremental time interval \( \Delta t \) in equation (5) with respect to the instantaneous condition of DC-link capacitor voltages \( V_{dc1} \) and \( V_{dc2} \). For example, if \( V_{dc1} - V_{dc2} \) is greater than or equal to the maximum allowable voltage deviation \( V_{d_{\text{max}}} \), \( T_{cp} \) are reduced while \( T_{cn} \) are increased accordingly to mitigate the sudden increased of voltage deviation. In contrast, if \( V_{dc1} - V_{dc2} \) is less than or equal to the minimum allowable voltage deviation \( V_{d_{\text{min}}} \), \( T_{cp} \) are increased while \( T_{cn} \) are reduced accordingly to cope with the sudden drop of voltage deviation. Meanwhile, if the neutral-point voltage deviation \( (V_{dc1} - V_{dc2}) \) falls within the allowable voltage deviation limit \( V_{d_{\text{min}}} \) and \( V_{d_{\text{max}}} \), \( \Delta t \) is set at 0.5 to maintain equal dwell time distribution for \( T_{cp} \) and \( T_{cn} \) respectively.

### V. RESULTS AND DISCUSSION

The three-phase three-level NPC inverter-based SAPF with the proposed neutral-point voltage deviation control algorithm is developed and tested in MATLAB / Simulink. The developed SAPF system is evaluated in term of the ability to mitigate the current harmonics present in the power system and the ability to minimize the neutral-point voltage deviation existing in NPC inverter. Two types of nonlinear loads are used for the testing purpose. The first nonlinear load is constructed using a three-phase uncontrolled bridge rectifier feeding a 20 \( \Omega \) resistor (resistive). The second nonlinear load is developed using similar rectifier feeding a series connected 50 \( \Omega \) resistor and 50 mH inductor (inductive). The details of the proposed parameters are summarized in Table III and Table IV. Furthermore, the SAPF system with conventional SVPWM algorithm stand-alone (without neutral-point voltage deviation control) is also tested for comparison purpose.

### TABLE III. PROPOSED PARAMETERS FOR SAPF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage source</td>
<td>400 Vrms, 50 Hz</td>
</tr>
<tr>
<td>DC-link capacitor</td>
<td>3300 ( \mu )F (each)</td>
</tr>
<tr>
<td>DC-link reference voltage</td>
<td>880 V</td>
</tr>
<tr>
<td>Limiting inductor</td>
<td>5 mH</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>25 kHz</td>
</tr>
</tbody>
</table>
Table IV summarizes the observation on the time taken for neutral-point voltage deviation control algorithm to successfully minimize the deviation which occurs in all nonlinear loads for different sets of $\Delta t$ values. It is clear that the best set of $\Delta t$ values is 0.9, 0.5, and 0.1 for the deviation condition of $V_{d_{\text{max}}} - V_{d_{\text{min}}} \geq V_d_{\text{max}}, V_d_{\text{min}} < V_{d_{\text{max}}}$, and $V_{d_{\text{max}}} - V_{d_{\text{min}}} \leq V_d_{\text{min}}$ respectively, where the time taken is the least for all nonlinear loads. Consequently, the stated set of values is applied in this work.

The simulation results of SAPF with the proposed algorithm which includes three-phase source voltage $v_s$, load current $i_L$, injection current $i_{inj}$, and source current $i_S$ for resistive and inductive loads are shown in Figure 3. Meanwhile, the THD values of the source current $i_S$ before and after connecting SAPF are summarized in Table V. The findings show that the current harmonics generated by all the nonlinear loads are successfully removed, resulting in THD value of below 5%, which complies with the limit set by IEEE Standard 519-2014 [15]. Furthermore, the mitigated source current $i_S$ seems to work in phase with the source voltage $v_s$ for all nonlinear loads, which leads to almost unity power factor.

On the other hand, Figure 4 shows the simulation results obtained for the overall DC-link voltage $V_{dc}$, the splitting capacitor voltages ($V_{d_{\text{ac}}} = V_{d_{\text{min}}}$, and $V_{d_{\text{ac}}} = V_{d_{\text{max}}}$), and neutral-point voltage deviation ($V_{d_{\text{ac}}} - V_{d_{\text{dc}}}$) for resistive and inductive loads. The findings show that SAPF without the proposed neutral-point voltage deviation control algorithm performs with a voltage deviation ranging from -3 to -5 V and 2 to 3 V for resistive and inductive loads respectively. However, when the proposed algorithm is activated at 3 s, the voltage deviation is further reduced to almost 0 V within a time delay of 0.05 s and 0.03 s for resistive and inductive loads respectively. Note that negative (-) sign refers to the inverse direction of voltage deviation. Moreover, voltages across the splitting capacitors ($V_{d_{\text{ac}}} = V_{d_{\text{min}}}$ and $V_{d_{\text{ac}}} = V_{d_{\text{max}}}$) for all the nonlinear loads are successfully maintained as half of the overall DC-link voltage $V_{dc}$, proving the effectiveness of proposed algorithm in minimizing the voltage deviation at neutral-point of NPC inverter.
In this paper, a simple yet effective neutral-point voltage deviation control algorithm for three-phase three-level NPC inverter-based SAPF is described and evaluated. The proposed algorithm serves as an enhancer to further improve the performance of SVPWM switching algorithm in balancing and minimizing the deviation of neutral-point voltage. As a result, the proposed algorithm has successfully controlled and reduced the neutral-point voltage deviation to a minimum level for all nonlinear loads. Most importantly, incorporation of the proposed algorithm has improved the performance of SAPF system in harmonics mitigation, where the current harmonics generated by all the nonlinear loads are successfully mitigated with THD value of far below 5%. The simulation results have confirmed the design concept and the effectiveness of the proposed neutral-point voltage deviation control algorithm.

VI. CONCLUSION

REFERENCES


